Remarks

This amendment is in response to the Office Action dated November 29, 2002. Claims 9-13, 15 and 17-20 have been amended. Claims 1-8 have been canceled without prejudice. Claims 9-21 are currently pending. Reexamination and reconsideration are respectfully requested.

Claims 1-7 have been canceled without prejudice as non-elected claims. Claim 8 has been canceled without prejudice and claim 9 has been rewritten in independent form. Dependent claims 10-13, 15 and 17-19 have been amended to depend from claim 9. Claim 20 has been amended to insert "annealing the first silicon oxide layer and the second silicon oxide layer at a temperature in the range of 600 – 850°C."

Claims 8-21 were rejected under 35 U.S.C. 102(e) as unpatentable over U.S. Patent No. 6,245,659 to Ushiyama et al. ("Ushiyama"). The rejection is respectfully traversed.

Applicant respectfully submits that the Examiner cited no portion of Ushiyama that describes a process including "the step of conducting an anneal treatment at a temperature of 600 – 850°C" as recited in independent claim 9. The Examiner cited Ushiyama at col. 12, lines 30-50. However, the portions cited by the Examiner appear to describe an annealing temperature of 350-500°C. Ushiyama at col. 12, lines 33-34. Such a range is substantially different than that recited in claim 9. Accordingly, applicant respectfully submits that the rejection should be withdrawn. The rejection of claims 10-19, which depend from claim 9, should be withdrawn for at least the same reasons as claim 9.

Independent claim 20 recites in part "annealing the first silicon oxide layer and the second silicon oxide layer at a temperature in the range of 600 – 850°C" and can be distinguished for at least similar reasons as for claim 9 discussed above. The rejection of claim 21, which depends from claim 20, should be withdrawn for at least the same reasons as claim 20.

Attached hereto is a marked-up version of the claim changes made by the present amendment. The attached page is captioned "Version with markings to show changes made."

Applicant respectfully submits that claims 9-21 are in condition for allowance. Reexamination and reconsideration are respectfully requested. If, for any reason, the application

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is not in condition for allowance, the Examiner is requested to telephone the undersigned to discuss the steps necessary to place the application into condition for allowance.

Respectfully submitted,

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Alan S. Raynes — March 31 , 2003

Alan S. Raynes **(Date)**

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Version With Markings to Show Changes Made

The paragraph at page 1, lines 6-10 was amended as follows:

Japanese Patent Application No. 2000-086607, filed March 27, 2000, is hereby incorporated by reference in its entirety. U.S. Patent Application Serial No. 09/817,935 [_____, entitled "Semiconductor Devices and Methods for Manufacturing the Same," invented by Kazumi Matsumoto, Yukio Morozumi, and Michio Asahina, having docket number 15.40/5753,] is hereby incorporated by reference in its entirety.

Claims 9-13, 15 and 17-20 were amended as follows:

9. (amended) A method for manufacturing a semiconductor device [according to claim 8, further] comprising [,] the steps of:

(a) forming a interlayer dielectric layer, the step including:

(a) (1) forming a first silicon oxide layer by reacting a silicon compound and hydrogen peroxide through a chemical vapor deposition method, and

(a) (2) forming a second porous silicon oxide layer by reacting a silicon compound, at least one of oxygen and a compound including oxygen, and a compound including an impurity through a chemical vapor deposition method;

(b) forming a wetting layer over the interlayer dielectric layer;

(c) forming a metal wiring layer over the wetting layer;

(d) forming a pad section by patterning the wetting layer and the metal wiring layer; and

after the step (a), the step of conducting an anneal treatment at a temperature of 600 – 850°C.

10. (amended) A method for manufacturing a semiconductor device according to claim 9 [8], wherein the silicon compound used in the step (a) (1) is at least one type selected

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from an inorganic silane compound including monosilane, disilane, SiH_2Cl_2 and SiF_4, or an organo silane compound including CH_3SiH_3, tripropyl-silane and tetraethylorthosilicate.

11. (amended) A method for manufacturing a semiconductor device according to claim 9 [8], wherein the step (a) (1) is conducted with the silicon compound being an inorganic silane compound by a reduced pressure chemical vapor deposition method at a temperature of 0 – 20°C.

12. (amended) A method for manufacturing a semiconductor device according to claim 9 [8], wherein the step (a) (1) is conducted with the silicon compound being an organo silane compound by a reduced pressure chemical vapor deposition method at a temperature of 100 – 150°C.

13. (amended) A method for manufacturing a semiconductor device according to claim 9 [8], wherein the step (a) (2) is conducted by a plasma chemical vapor deposition method at a temperature of 300 – 450°C.

15. (amended) A method for manufacturing a semiconductor device according to claim 9 [8], wherein the step (a) (2) is conducted by a chemical vapor deposition method at a temperature of 300 – 550°C.

17. (amended) A method for manufacturing a semiconductor device according to claim 9 [8], wherein, before forming the second silicon oxide layer in the step (a) (2), the first silicon oxide layer is exposed to an ozone atmosphere.

18. (amended) A method for manufacturing a semiconductor device according to claim 9 [8], wherein the impurity used in the step (a) (2) is phosphorous.

19. (amended) A method for manufacturing a semiconductor device according to claim 9 [8], wherein the metal wiring layer is provided by forming a first aluminum layer

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including aluminum or an alloy containing aluminum as a main component at a temperature of 200°C or lower, then forming a second aluminum layer including aluminum or an alloy containing aluminum as a main component at a temperature of 300°C or higher.

20. (amended) A method for manufacturing a semiconductor device, comprising:

forming a first silicon oxide layer using a polycondensation reaction of a silicon compound and hydrogen peroxide;

forming a second silicon oxide layer including an impurity therein;

annealing the first silicon oxide layer and the second silicon oxide layer at a temperature in the range of 600 – 850°C; and

forming a pad section over the first silicon oxide layer and the second silicon oxide layer, the pad section including a wetting layer and a wiring layer.

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